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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,609	05/18/2004	William Wang	12790-US-PA	3608

31561 7590 12/04/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VIDWAN, JASJIT S	
ART UNIT	**PAPER NUMBER**
2182	

NOTIFICATION DATE	DELIVERY MODE
12/04/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/709,609	WANG, WILLIAM	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/02/2007 has been entered.

Response to Arguments

2. Applicant's arguments filed 10/02/2007 have been fully considered but they are not persuasive. Applicant argues that prior art of record fails to teach "managing an address mapping table which is the cross reference between an access address transmitted from said data generation device and a physical address of storing the data in said data storage device."

3. With respect to above argument, **Examiner disagrees**. In arguments filed on 10/02//2007, Applicant contests that **despite Pattisam clearly stating** "...microprocessor issues starting and ending addresses to SCSI interface logic," the above fact is simply not true. Applicant provides unrelated excerpts from Pattisam's disclosure with regards to Compression coprocessor 220 and the application interface logic 215 and their respective functions. However, without establishing any relevance in connecting the functions of Compression coprocessor and the application interface logic to why the Applicant believes that Pattisam does not teach microprocessor issuing starting and ending addresses to SCSI interface logic (which Pattisam clearly himself states that he does), Applicant submits that "in light of the foregoing, Pattisam's microprocessor does not issue the starting and ending addresses to the compression coprocessor..." Regretfully so, Examiner is unable to follow the logic applied by the Applicant with respect to correlating the function of microprocessor in view of providing addresses to the SCSI interface with that of the compression coprocessor and interface logic.

4. In fact, in office action mailed on 08/02/2007, Examiner had directed Applicant's attention to Pattisam Col. 15, Lines 42-45 that read "Microprocessor issues starting and ending addresses to SCSI interface logic 260..." in support of the argument that in Pattisam's system, the microprocessor already

has control of providing address locations for the physical storage devices (280). Understanding that the microprocessor is responsible for providing the addressing of data storage space of 280, it would follow that microprocessor would be also responsible for "managing" the said data space. More specifically, when a host (200) requests given data (by either providing actual physical address or virtual address of said data), the microprocessor (230) processes the request by matching the address provided with the actual physical address of said data in question. Therefore, in fact the microprocessor is responsible for managing the addressing of the data storage. Furthermore, it is for this reason that it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Pattisam with that of Karpoff in order to provide that the cross referencing that Pattisam teaches is managed by way of an address mapping table in order to alleviate the host from being additionally responsible for managing the address mapping of the storage disk. In view of the above response, it is the position of the Examiner that the prior art still reads on the claimed invention.

5. With reference to the limitation of "mapping table" providing the cross-reference for address transfer. Examiner submits that the primary reference does not teach the mapping table with regard to the cross reference between an access address transmitted from host to physical address of the storage device. However since Pattisam teaches the microprocessor, as discussed above, as being responsible for providing physical address of the storage device it would be obvious in light of combination with Karpoff to utilize Karpoff's mapping table to handle the data addressing from the logical address provided by the host to the physical address of the storage device and vice versa. Further, Applicant argues that mapping table disclosed by Karpoff is **"not equipped with the function of address transmission based on the storage capacity before or after data compression proceeds."** However, it should be noted that claims as presented do not require the mapping table to be equipped with the function of address transmission before or after data compression. Though the Applicant submits that applicant's mapping table is equipped to handle the above functionality, the claim language does not require the above limitation as currently presented.

6. On a separate note, Examiner notes that the claims have not been amended since the last Final rejection was issued and therefore a first action FINAL would be proper. However, Examiner would like to

give an Applicant a fair opportunity to respond to the above arguments as presented by the Examiner. If the Applicant would like any further clarification on the Examiner's position or to discuss possible means to further the prosecution, Examiner invites the Applicant to contact the Examiner at the provided contact information at the end of the present action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pattisam et al, U.S. Patent No: 5,357,614 **[herein after Pattisam]** and further in view of Karpoff et at U.S. Patent No: 6,857,059 **[herein after Karpoff]**.

1. **As per Claim 1**, Pattisam teaches a data compression/decompression device **[see Fig. 3, element 20, *"Data compression controller"*]**, suitable for compressing/decompressing **[see Col. 2, Lines 48-52** – *the 'Data compression controller' decompresses data as well*] a data transmitted between a data generation device **[see Fig. 3, element 200, *"Host or I/O channel"*]** and a data storage device **[see Fig. 3, element 280, *"SCSI Devices"* – Also Col. 2, Lines 27-29** – *SCSI Device could be storage device*], comprising:

(a) Input buffer **[see Fig. 3, elements 210 & 211]**, for buffering and storing said data for input **[see Col. 11, Lines 58-60]**

(b) Output buffer **[see Fig. 3, elements 250]**, for buffering and storing said data for output **[see Col. 12, Lines 35-36]**

(c) Data compressor/decompressor **[see Fig. 3, elements 220, "Data compression coprocessor"]**, coupled to said output buffer **[Fig. 3, elements 213** – *Output data buffer is coupled to data compression coprocessor through compressed data bus 213*], for compressing/decompressing said data for input and storing said data for output in said output buffer **[see Col. 2, Lines 50-52]**

(d) Controller **[see Fig. 3, element 230, "Microprocessor"]**, coupled to said input buffer, said output buffer and said data compressor/decompressor, for controlling data transmission with said data generation device and said data storage device controlling compressing/decompressing said data **[Col. 8, Lines 44-58**, *Microprocessor employs Data Comp coprocessor interface logic to control compression coprocessor*]

Pattisam teaches the above limitations in addition to teaching a system wherein the microprocessor issues starting and ending addresses to SCSI interface logic for the data located in the data buffer (compressed data from host) **[see Col. 15, Lines 41-45]**. Pattisam goes further to disclose a system wherein the SCSI controller interface logic after receiving the starting and ending addresses from the microprocessor further identifies the addresses of the said data to the SCSI controller which is written to external device (storage devices) **[Col. 12, Line 63 – Col. 13. Line 1]**. Therefore, it follows that Pattisam teaches a microprocessor, which manages data addresses, issued by the host with that of physical address of storing the data in said data storage device (via use of SCSI interface logic and SCSI controller). However despite the above teachings, Pattisam fails to expressly teach performing the above function by way of "address mapping table" which is the cross reference between an access address transmitted from data generation device and physical address of storing the data in said data storage device.

Karpoff teaches the above deficiency by teaching a system wherein the microprocessor manages the mapping table which is the cross reference between an access address transmitted from data generation device (host) and a physical address of storing the data in data storage device **[see Karpoff, Col. 4, Lines 23-36]**. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the two teachings in order to take advantage of having a system where

the host application never has to deal with volume resizing and spare capacity can be amortized across multiple disk images, thus lowering the cost associated with "on reserve" storage capacity **[see Karpoff, Col. 3, Lines 46-64]**

2. **As per Claim 5**, Pattisam as modified by Karpoff above teaches a data compression/decompression device, comprising:

(a) Data storage device **[see Fig. 3, element 280**, ***"SCSI Devices"*** **– Also Col. 2, Lines 27-29 –** *SCSI Device could be storage device***]** having a data transmission interface **[Fig. 3, elements 260 & 270 – "SCSI controller Interface Logic" & "SCSI controller"]**

(b) Data generation device **[see Fig. 3, element 200,** ***"Host or I/O channel"*****]**, accessing a data in said data storage device via said data transmission interface **[see Col. 2, Lines 48-52]**; and a data compression/decompression device coupled to said data storage device and said data generation device via said data transmission interface **[see Fig. 3, element 20,** ***"Data compression controller"*****]**, for compressing/decompressing said data transmitted between said data storage device and said data generation device **[Col. 4, Lines 17-24]** and managing an address mapping table which is the cross reference between an access address transmitted from said data generation and a physical address of storing said data storage device **[see Karpoff, Col. 4, Lines 23-36]**

3. **As per Claim 2 and 7**, Pattisam as modified by Karpoff above teaches a device wherein said controller includes:

(a) Data generation control unit **[see Fig. 3, element 215, "Command/Data Registers Application Interface Logic"]**, for controlling data transmission with said data generation device

(b) Data storage control unit **[Fig. 3, element 260, "SCSI controller Interface Logic"]**, for controlling data transmission with said data storage device

(c) Data extractor, for obtaining said data from said input buffer, extracting a compressing/decompressing portion of said data, and sending said

compression/decompression portion of said data to said data compressor / decompressor **[Fig. 3, element 216, "Data Comp coprocessor Interface Logic"]**

(d) Main control unit for coordinating and controlling said data generation control unit, said data storage control unit, and said data extractor, and for managing said address mapping **[Fig. 3, element 230, "Microprocessor"]**

4. **As per Claim 3 and 8**, Pattisam as modified by Karpoff above teaches a device wherein said data generation device is at least one of a host, a laptop computer, a microprocessor, an interface card and a router **[see Fig. 3, element 200, *"Host or I/O channel"*]**

5. **As per Claim 4 and 9,** Pattisam as modified by Karpoff above teaches a device wherein said data storage device is at least one of a hard disk drive, floppy disk drive, a CD-RW drive, a magnetic-optical device, a digital video recorder and a flash memory card **[see Col. 4, Lines 5-9, "...SCSI compatible device specifically a tape drive, for storage of data in a compressed format"]**

6. **As per Claim 6**, *see rejection of Claim 1 above*

7. **As per Claim 10**, Pattisam as modified by Karpoff above teaches wherein said data transmission interface is one of an IDE interface, 1394 interface, a SCSI interface **[see Fig. 2, element 270]**, a serial interface, a serial attached SCSI interface, a PCMCIA interface and a USB interface.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
10/15/07

KIM HUYNH
SUPERVISORY PATENT EXAMINER
10/24/07